Elex / sem VI / 23/12/16 / CBGS
Basic VLSI design

Q.P. Code : 591602

(3 Hours) **[Total Marks :80**

N.B. : (1) **Question** No.**1** is compulsory.
(2) Solve any **three** questions from the remaining questions
(3) Assume suitable data if necessary

1. Solve any **four** of the following. **20**
   (1) Explain CMOS inverter characteristic mentioning all regions of operation.
   (2) Draw and explain AND gate using pass transistor logic
   (3) Implement 4 x 4 barrel shifter.
   (4) What are various programming techniques used for EEPROM.
   (5) Implement following function using CMOS.
   $F = A\,\overline{B} + \overline{A}\,\overline{C} + AB$

2. (a) Define scaling. Explain various types of scaling in detail. **10**
   (b) Explain clock skew and describe techniques to minimize it. **10**

3. (a) Draw 6T SRAM cell and explain it's read & write operation. **10**
   (b) Draw Dand JK latch using CMOS transmission gate and explain the working. **10**

4. (a) Explain latch up in CMOS in detail. What are remedie to avoid it. **10**
   (b) Compare Ripple carry adder and carry look ahead adder. Explain 4 bit CLA adder implementation. **10**

5. (a) What is ESD protection ? Explain in detail. **10**
   (b) Explain different clock generation schemes. Explain one clock distribution scheme in detail. **10**

6. Write short notes on: **any 4** **20**
   (a) Decoder circuits for ROM array
   (b) Inter connect scaling
   (c) Comparison of pseudo NMOS, Dynamic Static CMOS logic
   (d) Array multiplier
   (e) Sense amplitier